BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G01L 9/00, H01L 21/306

A1

(11) International Publication Number: **WO 95/16192**

(43) International Publication Date: 15 June 1995 (15.06.95)

(21) International Application Number: PCT/SE94/01181

(22) International Filing Date: 8 December 1994 (08.12.94)

(30) Priority Data:
9304145-7 10 December 1993 (10.12.93) SE

(71) Applicant *(for all designated States except US)*: PHARMACIA BIOTECH AB [SE/SE]; S-751 82 Uppsala (SE).

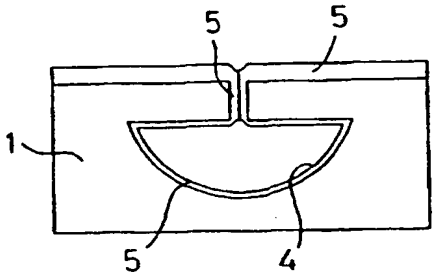
(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: ELDERSTIG, Håkan [SE/SE]; Nockeby Torg 12, S-161 41 Bromma (SE).

(74) Agents: WIDÉN, Björn et al.; Pharmacia AB, Patent Dept., S-751 82 Uppsala (SE).

(81) Designated States: JP, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
In English translation (filed in Swedish).

(54) Title: METHOD OF PRODUCING CAVITY STRUCTURES



(57) Abstract

A method of producing sealed cavity structures in the surface layer of a selectively etchable substrate (1), comprises: a) depositing a masking layer (2) of etchable material on the substrate (1), b) by means of etching, opening at least one hole (3) in the masking layer (2) down to the substrate surface, c) through said hole or holes (3) in the masking layer (2) selectively etching the substrate (1) in under the masking layer (2) so as to form one more cavities (4) which extend under the masking layer, and d) sealing said hole or holes (3) in the masking layer (2).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

METHOD OF PRODUCING CAVITY STRUCTURES

The present invention relates to a method of producing cavity structures, suitable for use as capillary fluid flow systems, pressure sensors etc., by means of micromechanical manufacturing methods.

One type of micromechanical manufacturing techniques is based upon microelectronic methods known from the semiconductor technology.

It is previously known to manufacture miniaturized analytical systems by means of microelectronic methods. For example, CH-A-679952 discloses the manufacture of an analytical chip, particularly for FIA (Flow Injection Analysis), by making channels in one or both of two plates of glass or silicon by photolithographic means, and then attaching the plates to each other such that a capillary system is defined between the two plates. The thickness of the plates reduces the possibilities of using microelectronic methods for integrating further functions in the system.

US-A-4,996,082 discloses a method of producing a cavity in a semiconductor substrate, particularly for use as a pressure sensor. In brief, the process consists in depositing onto a semiconductor substrate, typically of crystalline silicon, an oxide layer to a depth equivalent to the height of the desired cavity, depositing a layer of polycrystalline silicon on top of the oxide layer, and then from uncoated side portions of the oxide layer etching out a cavity under the layer of polycrystalline silicon. The etch channel openings can then be sealed by subjecting the substrate to an oxidizing ambient which results in growth of silicon dioxide in the channels sufficient to seal off the channels. Due to the need of etching from a side edge in under the substrate surface, the process is time-consuming and complicated.

The present invention provides a simplified and improved method of producing cavities of various types under the surface of an etchable substrate.

More particularly, the invention provides a method of producing sealed cavity structures in the surface layer of a selectively etchable substrate by:

a) depositing a protective layer, or masking layer, of etchable material on the substrate,

b) by means of etching, opening at least one hole in the masking layer down to the substrate surface,

c) through said hole or holes in the masking layer selectively etching the substrate in under the masking layer so as to form one or more cavities which extend under the masking layer, and

d) sealing said hole or holes in the masking layer.

The substrate material is preferably glass, quartz or silicon, while the masking layer preferably is polycrystalline silicon (polysilicon) or silicon nitride.

In one embodiment, the masking layer is polysilicon, and the sealing of the opening or openings in the masking layer is effected by oxidation of polysilicon to silicon dioxide, causing expansion of the polysilicon layer. Preferably, the substrate is of quartz, so that the whole finished product after the oxidation is totally of quartz.

In another embodiment, the sealing is effected by deposition of a material layer on the substrate surface and the hole walls. The deposited material may be a metal, a semiconductor or an insulator. The deposition may, for example, take place by sputtering, vaporization or a CVD (Chemical Vapor Deposition) method. If the substrate is of glass or quartz and the deposited material is silicon dioxide (quartz), a product that completely consists of quartz may be obtained.

In a further embodiment, the sealing of the opening or openings is effected by a combination of oxidation of a masking layer of polysilicon and deposition of an additional material layer.

The shape of the holes in the masking layer may vary depending on the desired cavity shape. As examples may be mentioned square and rectangular holes. A continuous cavity

can be made in the substrate via etching of a plurality of holes in the masking layer arranged adjacent to each other.

In the following, the invention will be described in more detail with reference to the accompanying drawing, where Figs. 1 to 5 schematically show different substeps in one embodiment of the method of the invention.

The chemical etching methods to which it will be referred below are well-known per se from inter alia the manufacture of integrated circuits (IC) and will therefore not be described in further detail here. It may, however, be mentioned that two basal etching phenomenons are used in micromachining, i.e. that (i) depending on substrate and etching agent, the etch may be dependent on the crystal direction or not, and (ii) the etch may take place selectively with regard to a specific material.

In a crystal direction dependent etch in a crystalline material, so-called anisotropic etch, etching is effected up to an atomic plane (111), which gives an extremely smooth surface. In a so-called isotropic etch, on the other hand, the etch is independent of the crystal direction.

The above-mentioned selectivity is based upon differences in etch rates between different materials for a particular etching agent. Thus, for the two materials silicon and silicon dioxide, etching with hydrogen fluoride takes place (isotropically) about 1,000 to about 10,000 times faster in silicon dioxide than in silicon. Inversely, potassium hydroxide gives an anisotropic etch of silicon that is about 100 times more efficient than for silicon dioxide, while a mixture of hydrogen fluoride and nitric acid gives a selective isotropic etch of silicon that is about 10 times faster than in silicon dioxide.

Now turning to the Figures, and with reference first to Fig. 1, one starts from a substrate 1, exemplified here by quartz. Onto the substrate is deposited a masking layer 2, exemplified here by polysilicon, in relation to which the substrate layer is selectively etchable. After application of photoresist and patterning in conventional manner, a hole 3 of a desired configuration is made in the

masking layer 2, as is shown in Fig. 2. In the illustrated case, it is assumed that a flow channel (capillary) is to be formed in the substrate, and the hole 3 is therefore oblong, e.g. 1 µm x 10 mm (with the longitudinal extension normal to the illustration plane).

With reference to Fig. 3, a selective etch of the substrate 1 is then carried out through the hole 3, here by way of example a wet etch with concentrated hydrogen fluoride, whereby the etch extends under the masking layer 2, so-called underetch. The etch is stopped when a cavity (here a flow channel) of the desired depth/width has been obtained.

The masking layer 2 of polysilicon is then oxidized to quartz, which causes the masking layer, including the walls of the hole 3, to expand, as illustrated in Fig. 4. Depending on the size of the hole 3, this oxidation step may optionally be sufficient for sealing the hole.

In the illustrated case, there still remains, however, as shown in Fig. 4, a small hole 3' in the masking layer 2. Complete sealing of the etched cavity or flow channel 4 is therefore effected, with reference to Fig. 5, by depositing a layer 5 of silicon dioxide (quartz). In the case contemplated here with a quartz substrate, the whole finished structure will therefore consist of quartz.

The substrate 1 in the above example may also be of glass, for example. In that case oxidation of polysilicon to quartz can, however, not be effected, since glass does not withstand the required oxidation temperature. Another alternative material is silicon (e.g. monocrystalline silicon). Furthermore, silicon nitride may be deposited instead of polysilicon as the masking layer 2.

In Figs. 3 to 5 the cavity (flow channel) 4 is illustrated as resulting from an isotropic etch. With an anisotropic etch of a silicon crystal, a cavity with a V-shaped profile would have been obtained instead, but without any underetch. Isotropic and anisotropic etching may, however, advantageously be combined in such a way that an isotropic etch of the substrate 1 is first carried out,

and the cavity walls are then smoothed in conformity with the crystal orientation by an anisotropic etch, so that the (111)-planes in the silicon crystal are etched out.

It is realized that on the whole just any desired sealed cavity structures can be manufactured by the process just described. The materials are selected with regard to the etch properties as well as the intended use of the finished product. Thus, capillaries may be made as above by opening an oblong hole in the etch mask. Alternatively, instead of an oblong hole, several holes in a row, e.g. square holes, may be made, such that a continuous capillary is formed along the row of holes under the etch mask by underetching the substrate for more than half the hole spacing.

Such capillaries may inter alia be used in chemical analysis systems. They may, for example, form liquid flow systems, e.g. for FIA (Flow Injection Analysis). Alternatively, they may form gas flow systems, e.g. for gas chromatography. A connection cup to a capillary may easily be provided by making a cavity adjacent to the capillary in the substrate. This is accomplished by means of a hole in the masking layer, which hole has a considerably greater lateral extension than the etch depth. In a chemical analysis system, it may sometimes be valuable to produce smooth flow channel walls by an anisotropic etch (optionally preceded by an isotropic etch) as described above, so that the channel walls may function as mirrors for certain applications of optical detection.

It is realized that by means of holes arranged adjacent to each other in the masking layer, it is possible to etch out continuous cavities of practically any shape and extension to suit a desired application.

For example, membranes may be produced according to the method of the invention by making a plurality of holes adjacent to each other, e.g. within a circle of a certain radius, for instance of a radius of about 0.1 mm, and then etching the substrate such that a continuous cavity is etched out under the masking layer. A membrane will then be

formed by the free part of the etch mask. Such a membrane may, for example, in combination with a strain gauge or a capacitive transducer be used as a pressure sensor. Another use of such a membrane is as a valve in gas or liquid flow systems. Still another use is for thermal insulation of, for example, a thermistor, e.g. for flow measuring.

Various desired components may easily be integrated in the cavity structures produced according to the invention. For example, electrodes can be integrated in a sealed cavity structure by opening a hole to an already prepared cavity, whereafter the hole is sealed by deposition of a metal layer which is then patterned and etched, so that electrodes are defined on the surface and brought into contact with the cavity. Such a cavity may, for example, be used for conductivity measurements or amperometric measurements. Alternatively, the electrodes are patterned on the substrate over the cavity to be formed before the production thereof, and holes are then made in the etch mask beside the electrodes and an underetch under the electrodes is performed. The holes are then sealed by depositing a thick layer over all of it. Then, the substrate layer under the electrodes is etched from within the cavity through openings thereto, so that the electrodes are brought into contact with the cavity.

When the substrate is a semiconductor material and the etch mask is an insulator, various electronic components, e.g. amplifiers, A/D converters, may in a similar manner be integrated on a substrate with a sealed cavity structure formed according to the method of the invention. For example, the substrate may be silicon while the etch mask may be silicon dioxide or silicon nitride.

Also, optical components may be integrated in the substrate for co-operation with the produced cavity structure. This applies to, for example, the integration of optical waveguides as doped (ion exchange) waveguides in the substrate bulk or as waveguides from glass, silicon nitride or a polymer. In this case the substrate suitably consists of glass.

In the following working example, the production of a flow channel according to the process of manufacture outlined in Figs. 1 to 5 will be described in more detail.

EXAMPLE

Production of a capillary on a quartz substrate

On a planar substrate of quartz, a 1 µm thick layer of polysilicon is deposited by LPCVD (Low Pressure Chemical Vapor Deposition). After application of photoresist and patterning of a number of holes in a row with a spacing of about 4 µm (alternatively a single oblong hole of the same length as the hole row), a hole or holes are etched in the polysilicon layer by means of RIE (Reactive Ion Etching). The photoresist is dissolved away, and a selective (isotropic) underetch of the quartz substrate through the holes (alternatively the oblong hole) with concentrated hydrogen fluoride for 5 min gives an about 5 µm deep and about 10 µm wide continuous cavity along the hole row (hole). By thermal oxidation of the polysilicon layer in water vapour, 950 °C, for 30 hours, all the silicon is then converted to silicon dioxide. Subsequent deposition of a 1.5 µm TEOS oxide (tetraethylorthosilicate oxide) then plugs the holes (hole) and forms a lid on the substrate. Then, a 0.5 µm layer of LTO (Low Temperature Oxide) with 4 % phosphorus is deposited. By heating at 1000 °C the phosphorus glass flows, whereby an almost smooth surface is obtained simultaneously as stresses in the glass disappear.

The invention is, of course, not restricted to the embodiments described above and specifically shown in the drawings, but many modifications and changes may be made within the scope of the following claims.

CLAIMS

1. A method of producing sealed cavity structures in the surface layer of a selectively etchable substrate, **characterized** by:

a) depositing a masking layer (2) of etchable material on the substrate (1),

b) by means of etching, opening at least one hole (3) in the masking layer (2) down to the substrate surface,

c) through said hole or holes (3) in the masking layer (2) selectively etching the substrate (1) in under the masking layer (2) so as to form one or more cavities (4) which extend under the masking layer, and

d) sealing said hole or holes (3) in the masking layer (2).

2. The method according to claim 1, **characterized** in that the substrate (1) is glass, quartz or silicon.

3. The method according to claim 1 or 2, **characterized** in that the masking layer (2) is polysilicon or silicon nitride.

4. The method according to claim 3, **characterized** in that the masking layer (2) is of polysilicon and the sealing step d) comprises oxidation of polysilicon to silicon dioxide and thereby expansion of the masking layer.

5. The method according to any one of claims 1 to 4, **characterized** in that the sealing of said holes (3) is effected by deposition of a material layer (5) on the substrate surface and the hole walls.

6. The method according to claim 5, **characterized** in that the deposited material layer is a metal, a semiconductor or an insulator.

7. The method according to claim 6, **characterized** in that the substrate is of glass or quartz and the deposited material is silicon dioxide.

8. The method according to claim 4, **characterized** in that the expansion of the masking layer (2) is sufficient for accomplishing the sealing of said hole or holes (3) therein.

9. The method according to claim 8, **characterized** in that the substrate is of quartz so that the product obtained is completely of quartz.

10. The method according to any one of the preceding claims, **characterized** in that the substrate (1) is a crystalline material and said cavity or cavities (4) in the substrate are formed by first performing an isotropic etch of the substrate and then an anisotropic etch.

11. The method according to any one of the preceding claims, **characterized** by making a plurality of holes (3) arranged adjacent to each other in the masking layer (2) and then through the holes (3) etching a continuous cavity (4) in the substrate (1).

12. The method according to any one of the preceding claims, **characterized** in that one or more of said holes (3) in the masking layer (2) are oblong.

13. The method according to any one of the preceding claims, **characterized** in that the substrate (1) is a semiconductor material and the masking layer (2) is an insulator.

14. The method according to any one of the preceding claims, **characterized** in that said cavity or cavities (3) comprise a capillary channel.

15. The method according to any one of the preceding claims, **characterized** in that the cavity structure (4) is a liquid or gas flow structure for a chemical analysis system.

16. The method according to any one of the preceding claims, **characterized** in that the cavity structure (4) forms a membrane structure.

17. The method according to any one of the preceding claims, **characterized** by integrating electrical, electronic and/or optical components in the sealed cavity structure.

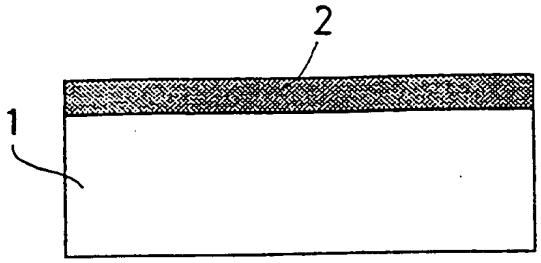


FIG. 1

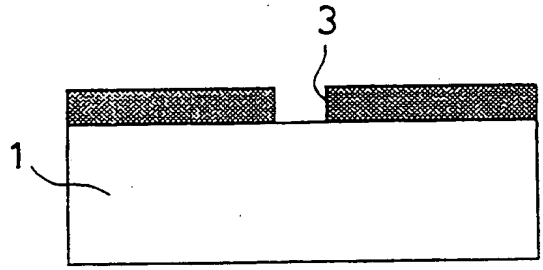


FIG. 2

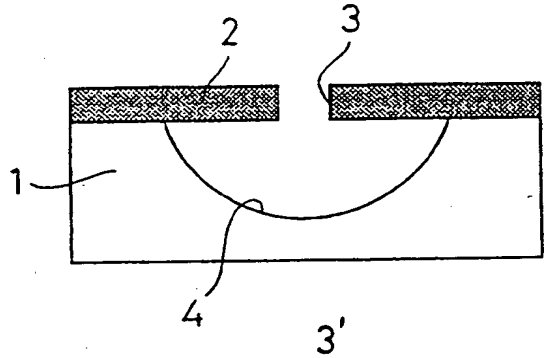


FIG. 3

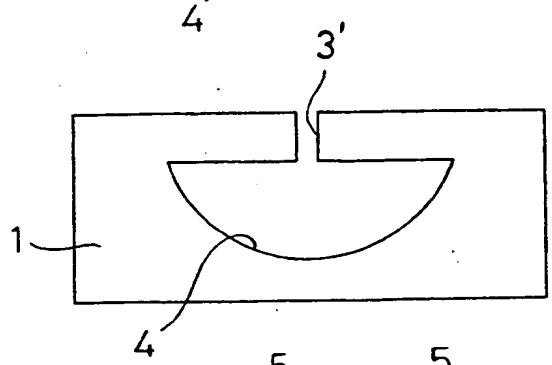


FIG. 4

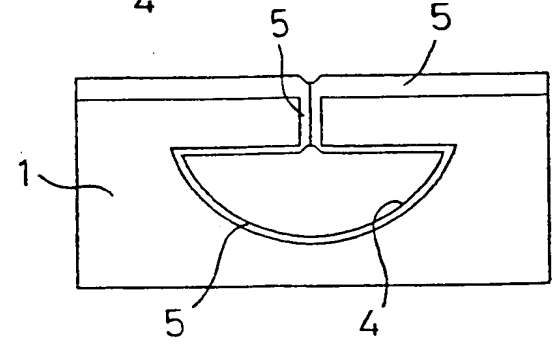


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 94/01181

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G01L 9/00, H01L 21/306
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G01L, H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Medicinsk Teknik, Volume, No 5, 1989, Bertil Hök et al, "Mikromekanik- här har kisel fått en ny roll" page 22	1,2,13,14,15
Y	--	1-7,9-17
Y	Proc. 3rd int. cong. solid-state sensor and actuators, Volume, June 1985, (Philadelphia), Petersen, K. et al, "High-precision, high-performance mass-flow sensor with integrated laminar flow micro-channels" page 361 - page 363	1-7,9-17
	--	
Y	EP, A1, 0566929 (ANT NACHRICHTENTECHNIK GMBH), 27 October 1993 (27.10.93), figures 1-11, abstract	1-7,9-17
	--	

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 March 1995	29 -03- 1995
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Lars Jakobsson Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 94/01181

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4885054 (M. SHIBAGAKI), 5 December 1989 (05.12.89), figures 1-11, abstract	1-7,9-17
Y	US, A, 3887404 (J.P. CHANE), 3 June 1975 (03.06.75), figures 1-3, abstract	1-7,9-17
Y	US, A, 3880684 (H. ABE), 29 April 1975 (29.04.75), figures 3,6-8, abstract	1-7,9-17
Y	Patent Abstracts of Japan, Vol 10,No 11, E-374, abstract of JP, A, 60-176239 (NIPPON DENKI K.K.), 10 Sept 1985 (10.09.85)	1-7,9-17
Y	Patent Abstracts of Japan, Vol 7,No 258, E-211, abstract of JP, A, 58-143535 (HITACHI SEISAKUSHO K.K.), 26 August 1983 (26.08.83)	1-7,9-17
Y	US, A, 5177661 (P.M. ZAVRACKY ET AL), 5 January 1993 (05.01.93), column 3, line 21 - column 5, line 4, figure 1	1,4,5,6
Y	US, A, 4908921 (F. CHEN ET AL), 20 March 1990 (20.03.90), figures 1,4, abstract	1,16
Y	US, A, 5127990 (D. PRIBAT ET AL), 7 July 1992 (07.07.92), figure 3, abstract	1,5

INTERNATIONAL SEARCH REPORT

Information on patent family members

25/02/95

International application No.
PCT/SE 94/01181

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A1- 0566929	27/10/93	NONE	
US-A- 4885054	05/12/89	JP-B- 1006276	02/02/89
		JP-C- 1522023	12/10/89
		JP-A- 62224687	02/10/87
US-A- 3887404	03/06/75	DE-A,C- 2303798	02/08/73
		FR-A,B- 2168936	07/09/73
		GB-A- 1417317	10/12/75
		JP-C- 1079228	25/12/81
		JP-A- 48085084	12/11/73
		JP-B- 56022136	23/05/81
US-A- 3880684	29/04/75	DE-A,C- 2340442	20/02/75
		FR-A,B- 2240526	07/03/75
		GB-A- 1398019	18/06/75
US-A- 5177661	05/01/93	US-A- 5095401	10/03/92
		EP-A- 0629286	21/12/94
		WO-A- 9318382	16/09/93
US-A- 4908921	20/03/90	DE-A- 3874470	15/10/92
		EP-A,A,A 0310225	05/04/89
		EP-A,A,A 0478093	01/04/92
		FI-C- 91328	10/06/94
		GB-A- 2211990	12/07/89
US-A- 5127990	07/07/92	DE-D,T- 68908638	23/12/93
		EP-A,B- 0350378	10/01/90
		FR-A- 2634059	12/01/90